

SELECTIVE SILICIDATION OF GATES IN SEMICONDUCTOR DEVICES
TO ACHIEVE MULTIPLE THRESHOLD VOLTAGES

TECHNICAL FIELD

[0001] The present invention relates to semiconductor devices and methods of manufacturing semiconductor devices. The present invention has particular applicability to double-gate devices.

BACKGROUND ART

[0002] The escalating demands for high density and performance associated with ultra large scale integration semiconductor devices require design features, such as gate lengths, below 100 nanometers (nm), high reliability and increased manufacturing throughput. The reduction of design features below 100 nm challenges the limitations of conventional methodology.

[0003] For example, when the gate length of conventional planar metal oxide semiconductor field effect transistors (MOSFETs) is scaled below 100 nm, problems associated with short channel effects, such as excessive leakage between the source and drain, become increasingly difficult to overcome. In addition, mobility degradation and a number of process issues also make it difficult to scale conventional MOSFETs to include increasingly smaller device features. New device structures are therefore being explored to improve FET performance and allow further device scaling.

[0004] Double-gate MOSFETs represent new structures that have been considered as candidates for succeeding existing planar MOSFETs. In several respects, the double-gate MOSFETs offer better characteristics than the conventional bulk silicon MOSFETs. These improvements arise because the double-gate MOSFET has a gate electrode on both sides of

the channel, rather than on only one side as in conventional MOSFETs. When there are two gates, the electric field generated by the drain is better screened from the source end of the channel. Also, two gates can control roughly twice as much current as a single gate, resulting in a stronger switching signal.

[0005] A FinFET is a recent double-gate structure that exhibits good short channel behavior. A FinFET includes a channel formed in a vertical fin. The FinFET structure may be fabricated using layout and process techniques similar to those used for conventional planar MOSFETs.

DISCLOSURE OF THE INVENTION

[0006] Implementations consistent with the present invention may provide a first FinFET device with a gate that is silicided a first amount and a second FinFET device with a gate that is silicided a second amount.

[0007] Additional advantages and other features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The advantages and features of the invention may be realized and obtained as particularly pointed out in the appended claims.

[0008] According to the present invention, the foregoing and other advantages are achieved in part by a semiconductor device that includes a substrate and an insulating layer formed on the substrate. A first device may be formed on the insulating layer. The first device may include a first fin formed on the insulating layer and a first silicided gate formed over a portion of the first fin. The first silicided gate may include a first thickness of silicide material. A second device also may be formed on the insulating layer. The second device may include a second fin formed on the insulating layer and a second silicided gate formed

over a portion of the second fin. The second silicided gate may include a second thickness of silicide material that is different from the first thickness.

[0009] According to another aspect of the invention, a method of manufacturing a semiconductor device may include forming first and second fin structures on an insulator and forming first and second gates over respective channel portions of the first and second fin structures. The method may also include partially siliciding the first and second gates and fully siliciding one of the first and second gates.

[0010] According to a further aspect of the invention, a semiconductor device may include a substrate and an insulating layer formed on the substrate. A first device may be formed on the insulating layer. The first device may include a first fin formed on the insulating layer, a first dielectric layer formed on the first fin, and a partially silicided gate formed over a portion of the first fin and the first dielectric layer. A second device also may be formed on the insulating layer. The second device may include a second fin formed on the insulating layer, a second dielectric layer formed on the second fin, and a fully silicided gate formed over a portion of the second fin and the second dielectric layer.

[0011] Other advantages and features of the present invention will become readily apparent to those skilled in this art from the following detailed description. The embodiments shown and described provide illustration of the best mode contemplated for carrying out the invention. The invention is capable of modifications in various obvious respects, all without departing from the invention. Accordingly, the drawings are to be regarded as illustrative in nature, and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Reference is made to the attached drawings, where elements having the same reference number designation may represent like elements throughout.

[0013] Fig. 1 is a cross-section illustrating exemplary layers that may be used for forming a fin in accordance with an embodiment of the present invention.

[0014] Fig. 2A schematically illustrates the top view of a fin structure in accordance with an exemplary embodiment of the present invention.

[0015] Fig. 2B is a cross-section illustrating the formation of the fin structure of Fig. 2A in accordance with an exemplary embodiment of the present invention.

[0016] Fig. 3 is a cross-section illustrating the formation of a gate oxide and gate material on the device of Fig. 2B in accordance with an exemplary embodiment of the present invention.

[0017] Fig. 4 is a cross-section illustrating the planarizing of the gate material of Fig. 3 in accordance with an exemplary embodiment of the present invention.

[0018] Fig. 5A schematically illustrates a top view of a FinFET structure in accordance with an exemplary embodiment of the present invention.

[0019] Fig. 5B is a cross-section illustrating the formation of the FinFET structure of Fig. 5A in accordance with an exemplary embodiment of the present invention.

[0020] Fig. 6 is a cross-section illustrating a further stage in the formation of the FinFET structure in accordance with an exemplary embodiment of the present invention.

[0021] Fig. 7 is a cross-section illustrating a further stage in the formation of some FinFET devices in accordance with an exemplary embodiment of the present invention.

[0022] Fig. 8 schematically illustrates a top view of a wafer including the devices of Figs. 6 and 7 in accordance with an exemplary embodiment of the present invention.

[0023] Figs. 9A to 9D are cross-sections illustrating the formation of a structure with a controlled thickness in a semiconductor device in accordance with another implementation of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0024] The following detailed description of the invention refers to the accompanying drawings. The same reference numbers in different drawings may identify the same or similar elements. Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims and their equivalents.

[0025] Implementations consistent with the present invention provide a first FinFET device with a gate that is silicided a first amount and a second FinFET device with a gate that is silicided a second amount. In one implementation, the second amount may be full silicidation of the gate. The different gate silicidation of the first and second devices may produce different threshold voltages for the devices.

[0026] Fig. 1 illustrates the cross-section of a semiconductor device 100 formed in accordance with an embodiment of the present invention. Although Fig. 1 and subsequent figures illustrate a single device 100, those skilled in the semiconductor arts will understand that other devices (e.g., semiconductor devices 100', 100'', etc. (see Fig. 8)) may be formed on the same wafer (or portion of a wafer, chip, etc.) in parallel with semiconductor device 100 using the process described herein. Referring to Fig. 1, semiconductor device 100 may include a silicon on insulator (SOI) structure that includes a silicon substrate 110, a buried oxide layer 120 and a silicon layer 130 formed on the buried oxide layer 120. Buried oxide layer 120 and silicon layer 130 may be formed on substrate 110 in a conventional manner.

[0027] In an exemplary implementation, buried oxide layer 120 may include a silicon oxide and may have a thickness ranging from about 1000 Å to about 3000 Å. Silicon layer 130 may include monocrystalline or polycrystalline silicon having a thickness ranging from about 300 Å to about 1500 Å. Silicon layer 130 is used to form a fin structure for a double-gate transistor device, as described in more detail below.

[0028] In alternative implementations consistent with the present invention, substrate 110 and layer 130 may include other semiconducting materials, such as germanium, or combinations of semiconducting materials, such as silicon-germanium. Buried oxide layer 120 may also include other dielectric materials.

[0029] A top dielectric layer 140, such as a silicon nitride layer or a silicon oxide layer (e.g., SiO₂), may be formed over silicon layer 130 to act as a protective cap during subsequent etching processes. In an exemplary implementation, dielectric layer 140 may be formed to a thickness ranging from about 150 Å to about 700 Å. Next, a photoresist material may be deposited and patterned to form a photoresist mask 150 for subsequent processing. The photoresist material may be deposited and patterned in any conventional manner.

[0030] Semiconductor device 100 may then be etched. In an exemplary implementation, dielectric layer 140 and silicon layer 130 may be etched in a conventional manner, with the etching terminating on buried oxide layer 120 to form a fin. Photoresist mask 150 may then be removed. After the formation of the fin, source and drain regions may be formed (e.g., by deposition or epitaxial growth of a semiconducting material) adjacent the respective ends of the fin. For example, in an exemplary embodiment, a layer of silicon, germanium or combination of silicon and germanium may be deposited, patterned and etched in a conventional manner to form source and drain regions. Alternately, the source and drain regions may be formed in the same photolithography process that forms the fin.

[0031] Fig. 2A schematically illustrates the top view of a fin structure on semiconductor 100 formed in such a manner. Source region 220 and drain region 230 may be formed adjacent the ends of structure 210 on buried oxide layer 120, according to an exemplary embodiment of the present invention.

[0032] Fig. 2B is a cross-section along line A-A' in Fig. 2A illustrating the formation of fin structure 210 in accordance with an exemplary embodiment of the present invention. As

described above, dielectric layer 140 and silicon layer 130 may be etched to form structure 210. Structure 210 may include a silicon fin 130 and a dielectric cap 140. In an exemplary implementation, the width of silicon fin 130 may range from about 10 \AA to about 100 \AA .

[0033] Fig. 3 is a cross-section illustrating the formation of a gate oxide and gate material on structure 210 in accordance with an exemplary embodiment of the present invention. A relatively thin gate oxide may be formed on exposed side surfaces of fin 130 as illustrated in Fig. 3. For example, a gate oxide 310 may be thermally grown on fin 130. Gate oxide 310 may be grown to a thickness of about 50 \AA to about 150 \AA and may be formed on the side surfaces of fin 130.

[0034] A gate material layer 320 may be deposited over semiconductor device 100 after formation of gate oxide 310. In an exemplary implementation, gate material layer 320 may include polysilicon deposited using conventional chemical vapor deposition (CVD) or other well known techniques. Alternatively, other semiconducting materials, such as germanium or combinations of silicon and germanium, or various metals may be used as the gate material in layer 320.

[0035] Fig. 4 is a cross-section illustrating the planarizing of gate material 320 in accordance with an exemplary embodiment of the present invention. Planarizing gate material 320 may remove any non-planar protrusions in the material, such as that shown above the fin structure 210 in Fig. 3. Returning to Fig. 4, chemical-mechanical polishing (CMP) or other conventional techniques may be performed so that the upper surface of gate material 320 is substantially planar. Planar gate material 320 may extend about 200 \AA to about 700 \AA above dielectric cap 140. A thickness of gate material 320 in the areas adjacent fin structure 210 after planarizing may range from about 700 \AA to about 2000 \AA .

[0036] Fig. 5A schematically illustrates the top view of semiconductor device 100 at one stage in processing in accordance with an exemplary embodiment of the present invention.

As illustrated, a gate may be patterned and etched in gate material 320 to form gate structure 510 that extends across a channel region of the fin structure 210.

[0037] Fig. 5B is a cross-section taken along line B-B' in Fig. 5A and illustrates the formation of semiconductor device 100 of Fig. 5A in accordance with an exemplary embodiment of the present invention. Gate structure 510 may be defined in gate material layer 320 by lithography (e.g., photolithography). A bottom antireflective coating (BARC) layer (not shown) may be deposited on planar gate material layer 320 to facilitate etching of gate material layer 320. As will be understood by those skilled in the semiconductor art, photoresist (and possibly a top antireflective (TAR) coating) may be deposited on the BARC layer and patterned in the shape of gate structure 510.

[0038] Gate material layer 320 (e.g., polysilicon) may then be selectively etched to form gate structure 510 out of gate material layer 320 on device 100. Planar gate material layer 320 may provide at least a planar bottom surface for the BARC layer (not shown), and may tend to flatten the top surface of the BARC layer. The BARC layer may have a thickness ranging from about 100 Å to about 500 Å. Because of planar gate material layer 320, the photoresist over the BARC layer may be patterned more precisely. As a result, the gate structure 510's critical dimension (CD) (i.e., its smallest feature size, such as the gate width) may be formed with dimensions as small as from about 20 nm to about 50 nm.

[0039] Gate structure 510 may include a gate portion proximate to the sides of the fin structure 210 and a larger electrode portion spaced apart from the fin structure 210. The electrode portion of gate structure 510 may provide an accessible electrical contact for biasing or otherwise controlling the gate portion.

[0040] As may be seen in Fig. 5B, portions of dielectric cap 140 located outside the perimeter of gate structure 510 may be removed. In other words, the selective etching of gate material layer 320 may remove all material beyond gate structure 510, down to fin 130 of fin

structure 210. Further, it should be noted that gate oxide 310 still may be present on fin 130, but is not illustrated in Fig. 5B because the line B-B' in Fig. 5A extends along fin 130 of fin structure 210.

[0041] The source/drain regions 220 and 230 may then be doped. For example, n-type or p-type impurities may be implanted in source/drain regions 220 and 230. The particular implantation dosages and energies may be selected based on the particular end device requirements. One of ordinary skill in this art would be able to optimize the source/drain implantation process based on the circuit requirements and such acts are not disclosed herein in order not to unduly obscure the thrust of the present invention. Activation annealing may then be performed to activate the source/drain regions 220 and 230.

[0042] Fig. 6 is a cross-section along the line B-B' in Fig. 5A illustrating a further stage in the formation of semiconductor device 100 in accordance with an exemplary embodiment of the present invention. Gate 510 may be "partially silicided" (i.e., silicided down to some thickness less than the full thickness of gate 510) to form partially silicided gate 600.

[0043] For such siliciding, a metal (e.g., nickel or cobalt) may be deposited over polysilicon gate 510. The metal may then be annealed to form silicided gate portion 610 (e.g., NiSi or CoSi₂) on polysilicon gate region 510 as illustrated in Fig. 6. In an exemplary implementation, the thickness of the silicided gate portion 610 may range from about 100 Å to about 1000 Å.

[0044] As noted above, other semiconductor devices may be formed on the same wafer (or portion of a wafer, chip, etc.) in parallel with semiconductor device 100 using the process described herein. In one implementation consistent with the principles of the invention, certain semiconductor devices may be covered by a mask, and further processing may be performed on those devices left uncovered by the mask. For example, some devices (e.g.,

device 100 in Fig. 6) may be covered with photoresist (or some other masking material) that is selectively removed to form a mask over these devices.

[0045] Fig. 7 is a cross-section illustrating a semiconductor device 100' that is left uncovered by such a mask. Semiconductor device 100' may initially have a partially silicided gate, like gate 600 of device 100 in Fig. 6. This gate may then be "fully silicided" (i.e., silicided down to dielectric cap 140) to form a fully silicided gate 700.

[0046] For such siliciding, a metal (e.g., nickel or cobalt) again may be deposited over the partially silicided gate. The metal may then be annealed to silicide any remaining polysilicon in gate 700 and form silicide material 710 (e.g., NiSi or CoSi₂) on dielectric cap 140 as illustrated in Fig. 7. In an exemplary implementation, the thickness of fully silicided gate 700 may range from 400 Å to about 1000 Å. After the full siliciding, the mask may be removed from the other semiconductor devices (e.g., device 100 in Fig. 6), and any further, typical processing may be performed on devices 100 and 100'.

[0047] Because of fully silicided gate 700, device 100' in Fig. 7 may have a different threshold voltage (V_t) than a similar device with a partially silicided gate (e.g., device 100 with gate 600 illustrated in Fig. 6). In one implementation consistent with the principles of the invention, fully silicided gate 700 may change the threshold voltage V_t of device 100' in Fig. 7 by about 200 mV to about 400 mV, relative to a device with a partially silicided gate (e.g., gate 600).

[0048] Fig. 8 schematically illustrates a top view of a wafer including device 100 (Fig. 6) and device 100' (Fig. 7) in accordance with an exemplary embodiment of the present invention. Buried oxide layer 120 illustrates the wafer (or chip), on which the three illustrated devices 100, 100' and 100'' are formed. Device 100 may have a partially silicided gate that is shown from above as silicided gate portion 610. Device 100' may have a fully silicided gate that is shown from above as silicide material 710. A third device 100'' may

have a gate 810 that is not silicided (e.g., as gate 510 in Fig. 5). Alternately, gate 810 may be partially silicided to a greater or lesser thickness than silicided gate portion 610 in device 100. Although devices 100, 100' and 100'' may be connected to other devices, or interconnected, these connections are not illustrated in Fig. 8 for clarity of presentation.

[0049] Those skilled in the art will understand, in view of the disclosure herein, that different devices (e.g., devices 100 and 100') may be formed with different V_t 's for a variety of design reasons. For example, the threshold voltage V_t may be varied based on the type of device 100/100'. In one implementation consistent with the principles of the invention, N-type MOS (NMOS) devices may be formed with a V_t larger in magnitude (i.e., absolute value) than the V_t of P-type MOS (PMOS) devices on the same wafer/chip. Alternately, PMOS devices may be formed with a V_t larger in magnitude than the V_t of NMOS devices on the same wafer/chip.

[0050] It may also be advantageous to vary V_t within a given circuit element (e.g., inverter, NAND gate, memory element, NOR gate, etc.). Within a single circuit element, for example, one FinFET device 100 may have a partially silicided gate 600 to achieve a first threshold voltage V_{t1} . Another FinFET device 100' within the circuit element may have fully silicided gate 700 and a second, different threshold voltage V_{t2} . In some implementations consistent with the principles of the invention, the fins of devices 100 and 100' in the circuit element may be electrically connected (e.g., by connecting region 230 in device 100 with region 220 in device 100' in Fig. 8).

[0051] Alternately, or additionally, V_t may be varied between circuit elements. For example, one circuit element may include one or more FinFET devices 100 having partially silicided gates 600 and associated first threshold voltages V_{t1} . A separate circuit element may include one or more FinFET devices 100' having fully silicided gates 700 and associated second, different threshold voltages V_{t2} .

[0052] Thus, in accordance with the present invention, different FinFET devices 100/100' may be formed with differentially silicided gates 600/700. These different devices 100/100' may be formed on the same wafer or chip and may exhibit different threshold voltages V_t . Advantageously, the resulting structure exhibits good short channel behavior. In addition, the present invention provides increased flexibility and can be easily integrated into conventional processing.

OTHER IMPLEMENTATION

[0053] In some implementations, it may be desirable to form a structure with a controlled thickness. Figs. 9A-9D are cross-sections illustrating the formation of a structure with a controlled thickness in a semiconductor device in accordance with another implementation of the present invention. Fig. 9A is a cross-section illustrating a FinFET 900 after fin formation (similar to Fig. 3). A silicon fin 930 may be formed on an insulator 920 and a substrate 910. Before fin 930 is formed a thin polish stop layer (PSL) may be deposited, resulting in a PSL cap 940 after fin formation. A polysilicon layer 950 may be deposited over the PSL cap 940 and fin 930 as shown in Fig. 9A.

[0054] Polysilicon layer 950 may be chemical-mechanical polished (CMP) until PSL cap 940 is reached (Fig. 9B). As this point, PSL cap 940 may produce materials that may be detected to stop the CMP. Use of PSL cap 940 may facilitate achieving a desired thickness of polysilicon layer 950 (e.g., 200 Å). The resulting polysilicon regions 950, however, are electrically disconnected. As illustrated in Fig. 9C, PSL cap 940 may then be removed, such as by selective etching.

[0055] Impurities may then be implanted into the structure of Fig. 9C, resulting in an implanted silicon layer 960 illustrated in Fig. 9D. Implanted silicon layer 960 may electrically connect polysilicon regions 950 on either side of fin 930. In this manner, polysilicon layer 950 may be formed with a thickness controlled by the height of fin 930.

Polysilicon regions 950 on either side of fin 930 may be re-connected using silicon implantation.

[0056] In the previous descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough understanding of the present invention. However, the present invention can be practiced without resorting to the specific details set forth herein. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention.

[0057] The dielectric and conductive layers used in manufacturing a semiconductor device in accordance with the present invention can be deposited by conventional deposition techniques. For example, metallization techniques, such as various types of CVD processes, including low pressure CVD (LPCVD) and enhanced CVD (ECVD) can be employed.

[0058] The present invention is applicable to the formation of any of various types of semiconductor devices, and hence, details have not been set forth in order to avoid obscuring the thrust of the present invention. In practicing the present invention, conventional photolithographic and etching techniques are employed and, hence, the details of such techniques have not been set forth herein in detail.

[0059] Only the preferred embodiments of the invention and a few examples of its versatility are shown and described in the present disclosure. It is to be understood that the invention is capable of use in various other combinations and environments and is capable of modifications within the scope of the inventive concept as expressed herein.

[0060] No element, act, or instruction used in the description of the present application should be construed as critical or essential to the invention unless explicitly described as such. Also, as used herein, the article "a" is intended to include one or more items. Where

only one item is intended, the term “one” or similar language is used. The scope of the invention is defined by the claims and their equivalents.